# EXP 3 – SHIFT RESISTER

library IEEE; use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

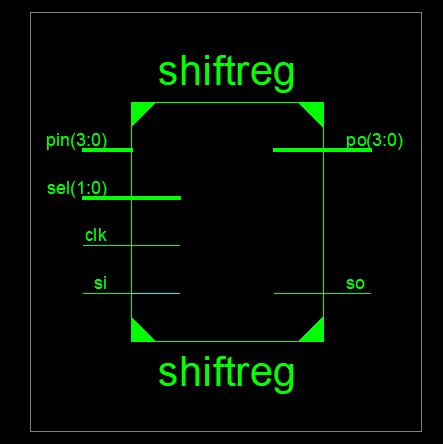
--use UNISIM.VComponents.all;

entity shiftreg is

Port ( si : in STD\_LOGIC; clk : in STD\_LOGIC; so : out STD\_LOGIC; pin : in STD\_LOGIC\_VECTOR (3 downto 0); po : out STD\_LOGIC\_VECTOR (3 downto 0); sel : in STD\_LOGIC\_VECTOR (1 downto 0)); end shiftreg; architecture Behavioral of shiftreg is signal temp:STD\_LOGIC\_VECTOR( 3 downto 0); begin process(clk) begin if(clk'event and clk='1')then case sel is

when"00"=> temp<= si&temp(3 downto 1);

so <=temp(3); when"01"=> temp<= si&temp(3 downto 1); po<=temp; when others=>null; end case; end if; end process; end Behavioral;



# TEST BENCH

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY shifttest IS

END shifttest;

ARCHITECTURE behavior OF shifttest IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT shiftreg PORT( si : IN std\_logic; clk : IN std\_logic; so : OUT std\_logic; pin : IN std\_logic\_vector(3 downto 0); po : OUT std\_logic\_vector(3 downto 0); sel : IN std\_logic\_vector(1 downto 0)

);

END COMPONENT; --Inputs

signal si : std\_logic := '0'; signal clk : std\_logic := '0'; signal pin : std\_logic\_vector(3 downto 0) := (others => '0'); signal sel : std\_logic\_vector(1 downto 0) := (others => '0');

--Outputs

signal so : std\_logic; signal po : std\_logic\_vector(3 downto 0); -- Clock period definitions constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT) uut: shiftreg PORT MAP ( si => si, clk => clk, so => so, pin => pin, po => po, sel => sel );

-- Clock process definitions clk\_process :process begin clk <= '0';

wait for clk\_period/2; clk <= '1';

wait for clk\_period/2;

end process; -- Stimulus process stim\_proc: process

begin

sel<="00"; si<='1';

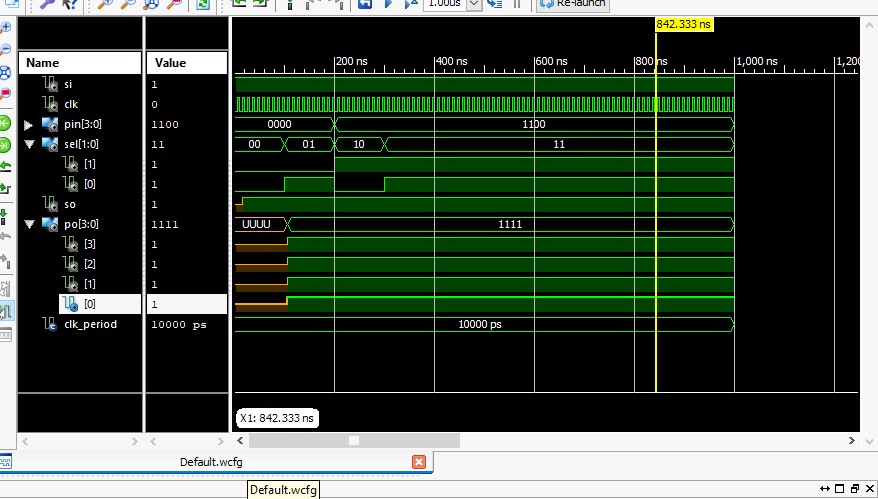
-- hold reset state for 100 ns.

wait for 100 ns;

sel<="01"; si<='1'; wait for 100 ns; sel<="10"; pin<="1100"; wait for 100 ns; sel<="11"; pin<="1100";

--=wait for clk\_period\*10; -- insert stimulus here wait; end process;

END;



# UCF FILE (SHIFT REGISTER)

NET clk LOC = P183;

NET Reset LOC = P102;

NET md(0) LOC = P101;

NET md(1) LOC = P100;

NET si LOC = P97;

NET so LOC = P156;

NET pi(0) LOC = P87;

NET pi(1) LOC = P86;

NET pi(2) LOC = P85;

NET pi(3) LOC = P81;

NET po(0) LOC = P162;

NET po(1) LOC = P165;

NET po(2) LOC = P166;

NET po(3) LOC = P167;

**Final Report**

Final Results

RTL Top Level Output File Name : shiftreg.ngr

Top Level Output File Name : shiftreg

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 13

Cell Usage :

# BELS : 6

# LUT2 : 2

# LUT3 : 4

# FlipFlops/Latches : 9

# FD : 4

# FDE : 5

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 8

# IBUF : 3

# OBUF : 5

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Device utilization summary:

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Selected Device : 3s400pq208-5

Number of Slices: 5 out of 3584 0%

Number of Slice Flip Flops: 9 out of 7168 0%

Number of 4 input LUTs: 6 out of 7168 0%

Number of IOs: 13

Number of bonded IOBs: 9 out of 141 6%

Number of GCLKs: 1 out of 8 12%

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Partition Resource Summary:

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No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-----------------------------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load | -----------------------------------+------------------------+-------+

clk | BUFGP | 9 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: 2.230ns (Maximum Frequency: 448.340MHz)

Minimum input arrival time before clock: 3.538ns

Maximum output required time after clock: 6.216ns

Maximum combinational path delay: No path found

Timing Detail:

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All values displayed in nanoseconds (ns)

# EXP 4 – MOD –N COUNTER

library IEEE; use IEEE.STD\_LOGIC\_1164.ALL; use IEEE.STD\_LOGIC\_unsigned.ALL; use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

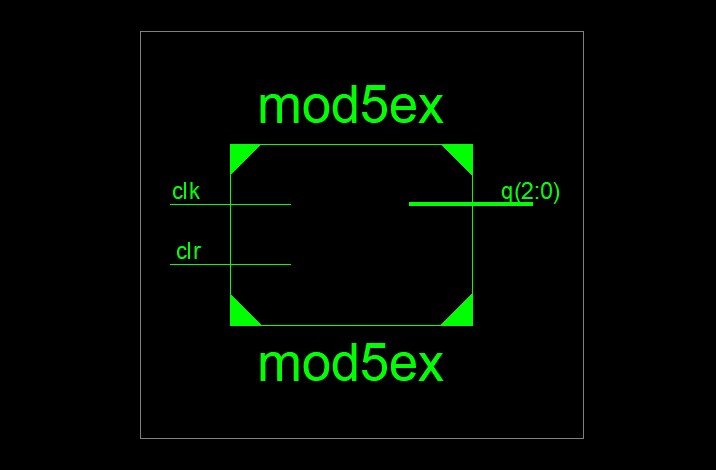
-- any Xilinx primitives in this code.

--library UNISIM; --use UNISIM.VComponents.all; entity mod5ex is

Port ( clk : in STD\_LOGIC; clr : in STD\_LOGIC; q : inout STD\_LOGIC\_VECTOR (2 downto 0)); end mod5ex; architecture Behavioral of mod5ex is signal count: std\_logic\_vector(2 downto 0); begin process(clk) begin if (clr='1') then count <= "000"; elsif (rising\_edge (clk)) then if (count="100") then count <= "000"; else

count<=count+ 1;

end if; end if; end process; q<=count; end Behavioral;



# TEST BENCH

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY mod5test IS

END mod5test;

ARCHITECTURE behavior OF mod5test IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT mod5ex PORT( clk : IN std\_logic; clr : IN std\_logic; q : INOUT std\_logic\_vector(2 downto 0)

);

END COMPONENT;

--Inputs signal clk : std\_logic := '0'; signal clr : std\_logic := '0';

--BiDirs

signal q : std\_logic\_vector(2 downto 0); -- Clock period definitions constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT) uut: mod5ex PORT MAP (

clk => clk, clr => clr, q => q );

-- Clock process definitions clk\_process :process begin

clk <= '0'; wait for 10 ns; clk <= '1'; wait for 10 ns;

end process;

-- Stimulus process stim\_proc: process

begin

clr<='1';

-- hold reset state for 100 ns.

wait for 20 ns;

clr<='0';

-- hold reset state for 100 ns.

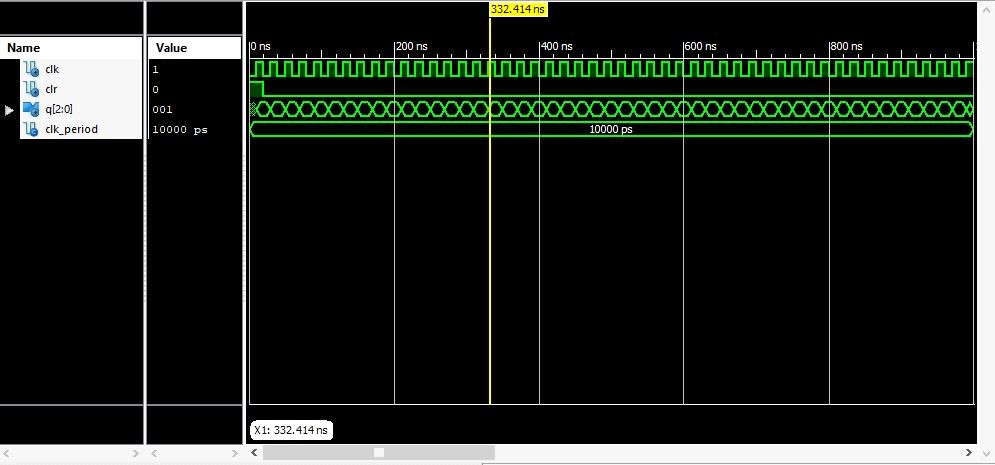
wait for 20 ns;

-- hold reset state for 100 ns.

-- wait for 100 ns;

-- wait for clk\_period\*10 -- insert stimulus here wait; end process;

END;



**Final Report**

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : mod5ex.ngr

Top Level Output File Name : mod5ex

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 5

Cell Usage :

# BELS : 3

# LUT2 : 1

# LUT3 : 2

# FlipFlops/Latches : 3

# FDC : 3

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 4

# IBUF : 1

# OBUF : 3

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Device utilization summary:

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Selected Device : 3s400pq208-5

Number of Slices: 2 out of 3584 0%

Number of Slice Flip Flops: 3 out of 7168 0%

Number of 4 input LUTs: 3 out of 7168 0%

Number of IOs: 5

Number of bonded IOBs: 5 out of 141 3%

Number of GCLKs: 1 out of 8 12%

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Partition Resource Summary:

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No Partitions were found in this design.

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# 

**EXP 5 – LCD**

library IEEE; use IEEE.STD\_LOGIC\_1164.ALL; use IEEE.STD\_LOGIC\_ARITH.ALL; use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity LCD\_SIMPLE\_Practice is Port ( rst,clk : in STD\_LOGIC; lcd\_RS : out STD\_LOGIC;

-- din : in std\_logic\_vector(7 downto 0); --LED : OUT std\_logic\_vector(7 downto 0); lcd\_EN : out STD\_LOGIC; data\_out : out STD\_LOGIC\_VECTOR (7 downto 0)); end LCD\_SIMPLE\_Practice;

architecture Behavioral of LCD\_SIMPLE\_Practice is signal div\_count : std\_logic\_vector(20 downto 0); signal clk\_new : std\_logic;

----------------------------------------------------------

type state is(reset,fuction,mode,cur,clear,d0,d1,d2,fuction1,mode1,cur1,clear1,d01,d11,d21); signal pss,nx : state; begin

--LED<=din;

-------------------------------------------------------------- clk\_DIV: process(clk,rst)

begin if rst= '1' then div\_count<= (others=>'0'); elsif clk'event and clk='1' then div\_count<= div\_count + '1'; end process;

-------------------------------------------------------------- clk\_new<= div\_count(20);

----------------------------------------------------------------

p\_state\_transactin: process (clk\_new,rst) begin if rst='1' then pss<=reset; elsif clk\_new'event and clk\_new= '1' then pss<= nx; end if;

end process;

------------------------------------------------------------------

LCD\_working: process(pss) begin case pss is

when reset =>

lcd\_RS<='0'; lcd\_EN<='1'; nx<= fuction;

data\_out<="00111100"; --3Ch

when fuction =>

lcd\_RS<='0'; lcd\_EN<='1'; data\_out<="00111100"; --3Ch nx<= fuction

when fuction1 =>

lcd\_RS<='0'; lcd\_EN<='0'; data\_out<="00111100"; --3Ch nx<= mode;

when mode =>

lcd\_RS<='0'; lcd\_EN<='1'; data\_out<="00000110"; --06h nx<= mode1;

when mode1 =>

lcd\_RS<='0'; lcd\_EN<='0'; data\_out<="00000110"; --06h nx<= cur;

when cur =>

lcd\_RS<='0'; lcd\_EN<='1'; data\_out<="00001100"; --0Ch nx<= cur1;

when cur1 => lcd\_RS<='0'; lcd\_EN<='0'; data\_out<="00001100"; --0Ch nx<= clear;

when clear => lcd\_RS<='0'; lcd\_EN<='1'; data\_out<="00000001"; --01h nx<= clear1;

when clear1 => lcd\_RS<='0'; lcd\_EN<='0'; data\_out<="00000001"; --01h

nx<= d0;

when d0 =>

lcd\_RS<='1'; lcd\_EN<='1'; data\_out<="01010011"; -----din; --S nx<= d01;

when d01 =>

lcd\_RS<='1'; lcd\_EN<='0';

data\_out<="01010011";-----din; --S

nx<= d1;

when d1 =>

lcd\_RS<='1'; lcd\_EN<='1'; data\_out<="01001011"; --K nx<= d11;

when d11 => lcd\_RS<='1'; lcd\_EN<='0'; data\_out<="01001011"; --K nx<= d2;

when d2 =>

lcd\_RS<='1'; lcd\_EN<='1'; data\_out<="01001110"; --N nx<= d21;

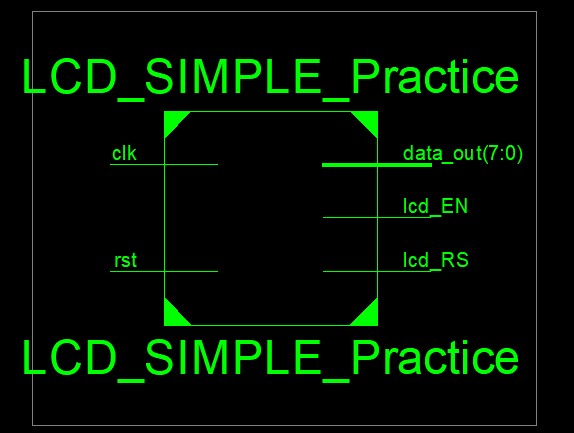
when d21 => lcd\_RS<='1'; lcd\_EN<='0'; data\_out<="01001110"; --N nx<= d21;

when others=>

null; end case;

end process;

end Behavioral;



# TEST BENCH

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY LCDTEST IS

END LCDTEST;

ARCHITECTURE behavior OF LCDTEST IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT LCD\_SIMPLE\_Practice PORT(

rst : IN std\_logic; clk : IN std\_logic; lcd\_RS : OUT std\_logic; lcd\_EN : OUT std\_logic; data\_out : OUT std\_logic\_vector(7 downto 0)

);

END COMPONENT;

--Inputs signal rst : std\_logic := '0'; signal clk : std\_logic := '0';

--Outputs

signal lcd\_RS : std\_logic; signal lcd\_EN : std\_logic;

signal data\_out : std\_logic\_vector(7 downto 0);

-- Clock period definitions constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT) uut: LCD\_SIMPLE\_Practice PORT MAP (

rst => rst, clk => clk, lcd\_RS => lcd\_RS, lcd\_EN => lcd\_EN, data\_out => data\_out

);

-- Clock process definitions clk\_process :process begin

clk <= '0';

wait for clk\_period/2; clk <= '1';

wait for clk\_period/2;

end process; -- Stimulus process stim\_proc: process begin rst<='1';

-- hold reset state for 100 ns.

wait for 100 ns; rst<='0';

--din<="00101010"; wait for 100 ns; rst<='1';

--din<="00101010";

-- hold reset state for 100 ns. rst<='0';

--din<="00101010"; wait for 100 ns; rst<='1';

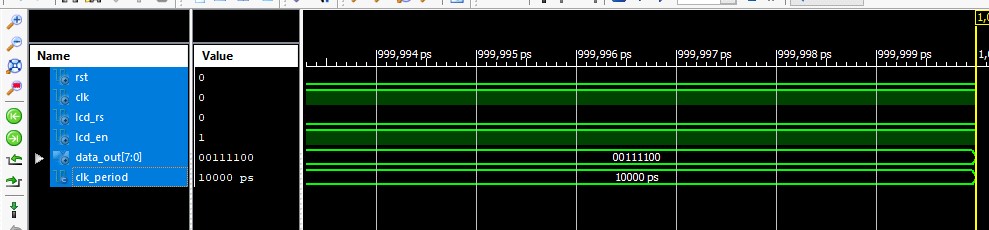
--din<="00111111";

--hold reset state for 100 ns.

wait for 100 ns; rst<='0'; wait for 100 ns;

-- insert stimulus here wait; end process;

END;



# UCF FILE (LCD)

NET data(0) LOC = P62;

NET data(1) LOC = P63;

NET data(2) LOC = P64;

NET data(3) LOC = P65;

NET data(4) LOC = P67;

NET data(5) LOC = P68;

NET data(6) LOC = P71;

NET data(0) LOC = P72;

NET clk LOC = P183;

NET reset LOC = P102;

**\* Final Report** \*

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Final Results

RTL Top Level Output File Name : LCD\_SIMPLE\_Practice.ngr

Top Level Output File Name : LCD\_SIMPLE\_Practice

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 12

Cell Usage :

# BELS : 83

# GND : 1

# INV : 1

# LUT1 : 20

# LUT2 : 2

# LUT3 : 5

# LUT4 : 11

# MUXCY : 20

# MUXF5 : 1

# VCC : 1

# XORCY : 21

# FlipFlops/Latches : 36

# FDC : 34

# FDCE : 1

# FDP : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 11 # IBUF : 1

# OBUF : 10

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Device utilization summary:

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Selected Device : 3s400pq208-5

Number of Slices: 23 out of 3584 0%

Number of Slice Flip Flops: 36 out of 7168 0%

Number of 4 input LUTs: 39 out of 7168 0%

Number of IOs: 12

Number of bonded IOBs: 12 out of 141 8% Number of GCLKs: 1 out of 8 12%

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Partition Resource Summary:

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No Partitions were found in this design.

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